

FPGA POWERLINK PE²MAC IP Core

Overview

The POWERLINK Enhanced Ethernet MAC Controller (PE²MAC) developed by *port* is a special MAC controller optimized for **Ethernet POWERLINK** for FPGAs. But nevertheless not only. It can handle standard TCP/IP as well and can be used for other protocols like Ethernet/IP™ or Modbus TCP.

Through several special transmit buffers and the possibility to respond automatically to POWERLINK frames by hardware, extremely short response times are reached. Special receive filters allow pre-filtering of POWERLINK messages by the MAC controller and releases the software from these tasks. These filters support the pre-selection of Ethernet frames, that are needed by the processing software. Based on the used settings only those frames that match the filters are stored in the receive buffers. This mechanism releases the CPU from processing frames not relevant for the software.

For the MAC unit a VHDL firmware design was developed that is optimized for POWERLINK data transfer.

Description

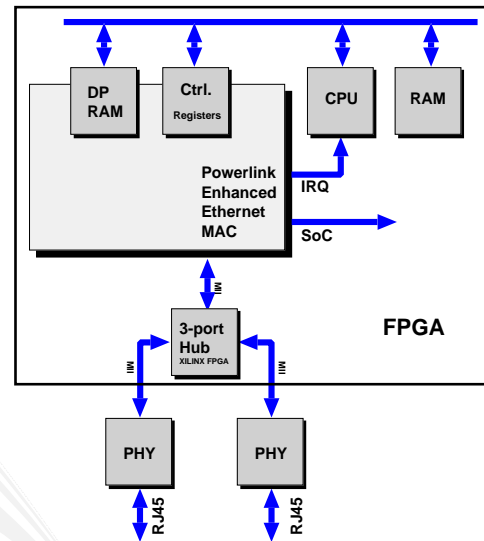
With FPGAs custom-made, scalable and future-proof solutions open up for the equipment manufacturer. The reusability of IPs, quick time to market and high cost efficiency, are substantial advantages of a FPGA based solution. E.g. a solution with Industrial Ethernet interface, hub logic and processor core can be implemented in one single XILINX-FPGA. Furthermore the embedded processor can directly be implemented in the FPGA.

The PE²MAC from *port* works in a Xilinx-FPGA and is available with three different processor interfaces:

- OPB or PLB v4.6 interface to connect to softcore processor MicroBlaze™
- a generic SRAM like interface for standalone solutions

The PE²MAC is a standalone component that is linked to the processor via registers (control- and status information), a dual-port-memory (data buffer) and an interrupt request signal. Furthermore a separated signal is provided that signals an incoming SoC packet.

A special PE²MAC driver provides an optimal interconnection to *port*'s POWERLINK Library.



In connection with the POWERLINK-HUB not only a straightforward connection to an POWERLINK network is provided but also a sophisticated solution with technical parameters (short response times, fast reaction to network events) that conforms to the requirements of the POWERLINK standard is available.

Technical Data

platform	Xilinx-FPGA
processor-connection	OPB, PLB v4.6 or SRAM
operation mode	100MBit
PHY interface	MII
Slices	1083 - 1238
FFs	952 - 1295
LUTs	1975 - 2161
BRAMs	6

Ordering Information

1712/00	PE ² MAC-XIL-OPB-VHDL
1712/01	PE ² MAC-XIL-PLB-VHDL
1712/02	PE ² MAC-XIL-SRAM-VHDL
1712/50	PE ² MAC-XIL-OPB-NETL
1712/51	PE ² MAC-XIL-PLB-NETL
1712/52	PE ² MAC-XIL-SRAM-NETL

Engineering Services

port is providing engineering services and trainings for our business activities:

- CAN and CAN-based protocols: CANopen, J1939, DeviceNet
- Industrial Ethernet Protocols: POWERLINK, EtherNet/IP, EtherCAT
- Implementation of devices according to CANopen device profiles
- VHDL based solutions for industrial applications
- application specific implementations or enhancements
- embedded LINUX projects

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